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Jack L. Lo, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, Dean M. Tullsen, S. J. Eggers August 1997 ACM Transactions on Computer Systems (TOCS), Volume 15 Issue 3

Full text available: pdf(526.39 KB)

Additional Information: full citation, abstract, references, citings, index terms, review

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Keywords: cache interference, instruction-level parallelism, multiprocessors, multithreading, simultaneous multithreading, thread-level parallelism

² A new guaranteed heuristic for the software pipelining problem

Pierre-Yves Calland, Alain Darte, Yves Robert

January 1996 Proceedings of the 10th international conference on Supercomputing

Full text available: pdf(892.93 KB) Additional Information: full citation, references, index terms

Keywords: circuit retiming, cyclic scheduling, guaranteed heuristic, list scheduling, software pipelining

AlphaSort: a RISC machine sort

Chris Nyberg, Tom Barclay, Zarka Cvetanovic, Jim Gray, Dave Lomet May 1994 ACM SIGMOD Record, Proceedings of the 1994 ACM SIGMOD international conference on Management of data, Volume 23 Issue 2

Full text available: pdf(1.17 MB)

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4 Special system-oriented section: the best of SIGMOD '94: AlphaSort: a cache-sensitive parallel external sort



Chris Nyberg, Tom Barclay, Zarka Cvetanovic, Jim Gray, Dave Lomet October 1995 The VLDB Journal — The International Journal on Very Large Data Bases, Volume 4 Issue 4

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings

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5 Adaptive two-level thread management for fast MPI execution on shared memory machines



Kai Shen, Hong Tang, Tao Yang

January 1999 Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM)

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6 Implementation of a parallel unstructured Euler solver on shared and distributed memory architectures



D. J. Mavriplis, R. Das, R. E. Vermeland, J. Saltz

December 1992 Proceedings of the 1992 ACM/IEEE conference on Supercomputing

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7 Gl-cube: an architecture for volumetric global illumination and rendering Frank Dachille, Arie Kaufman

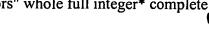


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Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing



A compilation-based software estimation scheme for hardware/software co-simulation Marcello Lajolo, Mihai Lazarescu, Alberto Sangiovanni-Vincentelli



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Keywords: compilation, delay modeling, software estimation

Application restructuring and performance portability on shared virtual memory and hardware-coherent multiprocessors

Dongming Jiang, Hongzhang Shan, Jaswinder Pal Singh

June 1997 ACM SIGPLAN Notices, Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 32 Issue 7

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Additional Information: full citation, abstract, references, citings, index terms

The performance portability of parallel programs across a wide range of emerging coherent shared address space systems is not well understood. Programs that run well on efficient, hardware cache-coherent systems often do not perform well on less optimal or more commodity-based communication architectures. This paper studies this issue of performance portability, with the commodity communication architecture of interest being page-grained shared virtual memory. We begin with applications that per ...

10 Compile/run-time support for threaded MPI execution on multiprogrammed shared memory machines



Hong Tang, Kai Shen, Tao Yang

May 1999 ACM SIGPLAN Notices, Proceedings of the seventh ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 34 Issue

Full text available: pdf(1.54 MB)

Additional Information: full citation, abstract, references, citings, index

MPI is a message-passing standard widely used for developing high-performance parallel applications. Because of the restriction in the MPI computation model, conventional implementations on shared memory machines map each MPI node to an OS process, which suffers serious performance degradation in the presence of multiprogramming, especially when a space/time sharing policy is employed in OS job scheduling. In this paper, we study compile-time and run-time support for MPI by using threads and dem ...

11 The Totem multiple-ring ordering and topology maintenance protocol D. A. Agarwal, L. E. Moser, P. M. Melliar-Smith, R. K. Budhia May 1998 ACM Transactions on Computer Systems (TOCS), Volume 16 Issue 2



Full text available: pdf(367.16 KB)

Additional Information: full citation, abstract, references, citings, index terms, review

The Totem multiple-ring protocol provides reliable totally ordered delivery of messages across multiple local-area networks interconnected by gateways. This consistent message order is maintained in the presence of network partitioning and remerging, and of processor failure and recovery. The protocol provides accurate topology change information as part of the global total order of messages. It addresses the issue of scalability and achieves a latency that increases logarithmically with ...

Keywords: Lamport timestamp, network partitioning, reliable delivery, topology maintenance, total ordering, virtual synchrony

12 A flexible operation execution model for shared distributed objects Saniya Ben Hassen, Irina Athanasiu, Henri E. Bal
October 1996 ACM SIGPLAN Notices, Proceedings of the 11th ACM SIGPLAN
conference on Object-oriented programming, systems, languages, and applications, Volume 31 Issue 10
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13 Session 4: communications libraries: SLICC: a low latency interface for collective
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Allan D. Knies, William J. Harrod, F. Ray Barriuso, George B. Adams November 1994 Proceedings of the 1994 ACM/IEEE conference on Supercomputing
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Several recent parallel computers have implemented logically shared, physically distributed memory systems which allow processors to directly access memory in other processors without interrupting the referenced PE. Because this kind of architecture provides greater flexibility for interprocessor communications than private address space computers, different software models can be developed to take advantage of these machines. In this paper, we describe a low-level collective communications inte
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Elizabeth Borowsky, Eli Gafni June 1993 Proceedings of the twenty-fifth annual ACM symposium on Theory of computing
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High performance synchronization algorithms for multiprogrammed multiprocessors Robert W. Wisniewski, Leonidas I. Kontothanassis, Michael L. Scott August 1995 ACM SIGPLAN Notices, Proceedings of the fifth ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 30 Issue 8
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April 1996 Communications of t	D. A. Agarwal, R. K. Budhia, C. A. Lingley-Papadopoulos	
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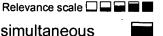
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Jack L. Lo, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, Dean M. Tullsen, S. J. Eggers August 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 3

Full text available: pdf(526.39 KB)

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Hong Tang, Kai Shen, Tao Yang

May 1999 ACM SIGPLAN Notices, Proceedings of the seventh ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 34 Issue

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12 Model refinement for hardware-software codesign

Jie Gong, Daniel D. Gajski, Smita Bakshi

January 1997 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 2 Issue 1

Full text available: pdf(436.53 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>, review

Hardware-software codesign, which implements a given specification with a set of system components such as ASICs and processors, includes several key tasks such as system component allocation, functional partitioning, quality metrics estimation, and model refinement. In this work, we focus on the model refinement task which transforms a specification from an original functional model to a refined implementation model. First, we categorize several commonly used implementation models and desc ...

Keywords: functional model, implementation model, model refinement, sofware-hardware codesign

13	An execution model for distributed object-oriented computation							
	Edward H. Bensley, Thomas J. Brando, Myra Jean Prelle							
	January 1988 ACM SIGPLAN Notices, Conference proceedings on Object-oriented							
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	This paper describes an execution model being developed for distributed object-oriented in a message-passing multiple-instruction/multiple-data-stream (MIMD) environment. The objective is to execute an object-oriented program as concurrently as possible. Some opportunities for concurrency can be identified explicitly by the programmer. Others can be identified at compile time. There are some opportunities for concurrency, however, that can only be discovered at runtime because they are data							
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... z/VM is running in a logical partition) processors available to ... This capability can

be extremely useful to test a guest ... z/VM is running in an LPAR, the logical ...

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... needs: - Logical partitioning (LPAR) - Client Access ... consolidation, mixed production/test

environments, and \dots **Processors**, memory, and interactive performance \dots

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... to meet the receiver value **test**, the next ... intervals Because adjusting logical **partition processor** weights can ... usage is understood by the **LPAR** cluster members ... www.research.ibm.com/journal/rd/464/rooney.html - 101k - Cached - Similar pages

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... allow for dynamic adjustment of logical partition processor weights ... relevant to WLM involvement in IRD LPAR CPU management ... to pass the receiver value test and is ...

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... certification was concluded with • the comparability test and • the ... the use of the machine in LPAR mode ... check-stopped - this state indicates that a physical ...

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... three (3) weeks to allow the Field Security Operations SRR team to complete its data ... Reference:

LPAR STIG 4.2.1.1. ... Check to see that a log exists and is used. ...

csrc.nist.gov/pcig/CHECKLISTS/lparcklst-v2r11jul03.doc - Similar pages

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... conditions is shown which were necessary to complete one SSCH ... TIME: 21.00.01 ACT:

POR MODE: LPAR CPMF: EXTENDED ... delivering up to 100 MB/sec, full-duplex data ...

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... BEST/1 Capacity Planning Tool **Manual** (SC41-3341 ... http://www.as400.ibm.com/lpar/sysdesign.htm ... Create

and Add Primary Partition Processor Memory Workload ...

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... No.1 0.4 shared processor 64MB memory No direct attach I/O Linux SECONDARY No.2 0.5 shared processor 100MB memory 1 Gbit Ethernet IOA **LPAR** Validation Tool (LVT ... www.common-d.de/pdf/Linux Partition.pdf - Similar pages

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... Up to 32 partitions LPAR on Selected ... processing units: Number of partition processors:

Partial Processors ... CPW Avail) / 1000 (1 partition processor) = .50 or 50 ...

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... on the control panel (key in manual position) 2 ... job doing 5250 OLTP processing) LPAR

does impose ... more 5250 capacity than the partition's processor capacity (Note ...

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... by the machine's Logical Partitioning (LPAR) support to ... This manual also describes

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... 6 DBLINUX Number of partition processors Press F10 to IPL the whole system now ... F3=Exit

F10=IPL system to activate changes F12=Cancel Some LPAR Config Changes ...

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... Information Technology Security Evaluation Manual (ITSEM), Version ... use of the machine

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...... 173 LPAR Performance 177 43. Shared LPAR

CP monitor data summary (percent, rounded to tenths) 180 44. ...

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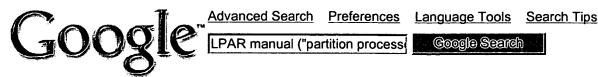
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... Finally, no system discussion would be complete without some ... Logical Storage Unit,

FXU = Fixed point (integer) Unit, BXU ... to the module, and the full L2 onboard ...

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... Logical Partition Environment The following is a brief explanation of the **LPAR** macro parameters. For more details see the SNAP/SHOT Input Reference **Manual** (S/S ...

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... business goals, WLM continuously adapts systems resources within an LPAR to actual ... parallel,

thus reducing the overall elapsed time for the query to complete. ...

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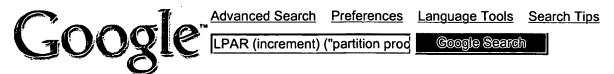


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